EXHIBIT A

Comparison of Original Claim 1 and Claim 2 and Amended Claim 1 and Claim 2

Original Claim 1 and Claim 2 (emphasis added)	Following Amendment
1. A method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature to a predetermined register of the first processor; executing in a first processor a command of a software application to cause the first processor to initiate a system management interrupt; receiving at each processor an instruction that a software system management interrupt has been issued; entering system management mode at each processor; saving the register contents of each processor to a memory space associated with each respective processor; selecting a second processor as the system management interrupt handler; scanning the contents of the memory space associated with each processor; and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt. 2. The method for issuing and handling system management interrupts in a multiprocessor computer system of claim 1, *wherein the step of selecting a second processor as the system management interrupt handler comprises the step of selecting a second processor as the system management interrupt handler according to an arbitration scheme.*	1. (Amended) A method for handling system management interrupts in a multiprocessor computer system, comprising the steps of: writing a predetermined signature to a predetermined register of ~~the~~ a first processor; executing in a the first processor a command of a software application to cause the first processor to initiate a system management interrupt; receiving at each processor an instruction that ~~a software~~ the system management interrupt has been issued; entering system management mode at each processor; saving ~~the~~ register contents of each processor to a memory space associated with each respective processor; selecting a second processor as ~~the~~ a system management interrupt handler, the selection of the second processor as the system management interrupt handler being accomplished according to an arbitration scheme; scanning the contents of the memory space associated with each processor; and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt. 2. (Cancelled).